Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1 - 20 (Cancelled).

21. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on the gate oxide film;

a source/drain region formed in the semiconductor substrate and disposed adjacent to the gate electrode;

a lower layer wiring connected to the source/drain region with contact;

an interlayer insulating film covering the lower layer wiring;

a via hole formed in an interlayer insulating film; and

an upper layer wiring ~~having a pad portion~~, disposed over the interlayer insulating film and connected to the lower layer wiring through the via hole,

wherein the upper layer wiring and the lower layer wiring are arranged under a pad portion and in areas other than under the pad portion, and

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion.

22. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on gate oxide film;

a source/drain region formed in the semiconductor substrate and disposed adjacent to the gate electrode;

a semiconductor region formed under the gate electrode comprising a channel;

a low concentration region of the same conductivity type as the source/drain region formed under the gate electrode so as to connect to the source/drain region and to contact the semiconductor region;

interlayer insulating film disposed over the gate electrode and the gate oxide film;

a lower layer wiring disposed in the interlayer insulating film and coupled to the source/drain region; and

an upper layer wiring disposed over the interlayer insulating film and coupled to the lower layer wiring through a hole in the interlayer insulating film.

23. (Previously Presented) A semiconductor device according to claim 21, further comprising:

a semiconductor region formed under the gate electrode, said region comprising a channel, wherein the low concentration region extends shallowly to a surface layer under the gate electrode to connect to the source/drain region and to contact the semiconductor region.

24 - 27. (Canceled)

28. (Previously Presented) The semiconductor device according to claim 21, wherein the interlayer insulating layer is provided with additional holes to couple the upper wiring to the lower layer wiring.

29-30. (Canceled)

31. (Previously Presented) The semiconductor device according to claim 21, further comprising a semiconductor region formed under the gate electrode and constituting a channel.

32. (Previously Presented) The semiconductor device according to claim 31, further comprising a bump electrode provided at the pad portion.

33. (Previously Presented) The semiconductor device according to claim 21, further comprising a bump electrode provided at the pad portion.

34. (Currently amended) A semiconductor device comprising:

a lower layer wiring;

an interlayer insulating film covering the lower layer wiring;

a via hole formed in the interlayer insulating film; and

an upper layer wiring ~~having a pad portion~~, disposed over the interlayer insulating film and connected to the lower layer wiring through the via hole,

wherein the upper layer wiring and the lower layer wiring are arranged under a pad portion and in areas other than under the pad portion, and

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion.

35. (Previously presented) The semiconductor device according to claim 34, wherein the interlayer insulating layer is provided with additional holes to couple the upper layer wiring to the lower layer wiring.

36. (Previously presented) The semiconductor device according to claim 34, further comprising a bump electrode provided at the pad portion.

37. (Previously presented) The semiconductor device according to claim 36, further comprising the lower layer wiring arranged below the bump electrode.

38. (New) The semiconductor device according to claim 21 wherein the pad portion comprises a bump electrode.

39. (New) The semiconductor device according to claim 34 wherein the pad portion comprises a bump electrode.